CLAIMS

Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows:

1. A method of providing programming of dual edge programmable delay unit comprising:

providing a buffer circuit which is adapted to receive a buffer input signal, with said buffer input signal falling at an input signal fall time and said buffer input signal rising at an input signal rise time;

said buffer circuit providing a falling buffer output signal at an output signal fall time and a rising buffer output signal at an output signal rise time;

providing a variable fall time control input;

providing a variable rise time control input;

providing a Fall Time Programmable Control Source (FTPCS) for programming a variable FTPCS signal to said buffer circuit as a function of said fall time control input;

providing a Rise Time Programmable Control Source (RTPCS) for programming a variable RTPCS signal to said buffer circuit as a function of said rise time control input;

said buffer circuit providing said buffer output signal with a fall time delay between said input signal fall time and said output signal fall time as a function of said variable FTPCS signal; and

said buffer circuit providing said buffer output signal with a rise time delay between said input signal rise time and said output signal rise time as a function of said variable RTPCS signal.

2. The method of claim 1 wherein said buffer circuit includes a first inverter and a second inverter.

3. The method of claim 1 including:

providing said buffer circuit with a first inverter and a second inverter;

providing for said first inverter to have an input for receiving said buffer input signal via an intermediate node;

providing for second inverter output to generate said buffer output signal in response to an input to a second inverter input;

providing for said first inverter to have a first inverter output connected to said second inverter input;

providing for said first inverter to respond to said FTPCS when said input signal transits from logic high to logic low to initiate said fall time delay;

providing for said first inverter to respond to said second RTPCS when said input signal transits from logic low to logic high to initiate said rise time delay;

generating triggering of said second inverter to initiate said falling buffer output signal at the end of said fall time delay and to initiate said rising buffer output signal at the end of a rise time delay.

4. The method of claim 3 including connecting a capacitor between said node and a reference potential.

5. The method of claim 3 including:

connecting a capacitor between said node and a reference potential; and

providing a Schmitt trigger circuit as said second inverter.

6. The method of claim 3 including providing for said buffer control circuit to respond as follows:

a. to an output current from said FTPCS when said input signal transits from logic high to logic low; and

b. to respond an output current through said RTPCS when said input signal transits from logic low to logic high.

7. The method of claim 3 including:

providing a first control word to a first latch which in turn provides a first variable control signal to said FTPCS; and

providing a second control word to a second latch which in turn provides a second variable control signal to said RTPCS.

8. The method of claim 7 including:

providing FET fingers in said FTPCS with each finger thereof being controlled by an output from a register in said first latch; and

providing FET fingers in said second RTPCS with each finger thereof being controlled by an output from a register in a corresponding latch.

9. The method of claim 3 including:

providing current mirror circuits in said FTPCS and said RTPCS;

providing a first control word to a first latch which in turn provides a first variable control signal to said first FTPCS;

providing a second control word to a second latch which in turn provides a second variable control signal to said RTPCS; and

providing FET fingers in said FTPCS with each finger thereof being controlled by an output from a register in said first latch; and

providing FET fingers in said RTPCS with each finger thereof being controlled by an output from a register in a corresponding latch.

10. The method of claim 9 including connecting a capacitor between said node and a reference potential.

11. The method of claim 9 including:

connecting a capacitor between said node and a reference potential; and

providing a Schmitt trigger circuit as said second inverter.

12. The method of claim 9 including providing current mirror circuits in said FTPCS and said RTPCS.

13. The method of claim 9 including:

providing a first control word to a first latch which in turn provides a first variable control signal to said FTPCS; and

providing a second control word to a second latch which in turn provides a second variable control signal to said RTPCS.

14. The method of claim 13 including:

providing FET fingers in said FTPCS with each finger thereof being controlled by an output from a register in said first latch; and

providing FET fingers in said RTPCS with each finger thereof being controlled by an output from a register in a corresponding latch.

15. A method of providing dual edge programming in a programmable delay unit comprising:

providing a buffer control circuit with a signal input, a signal output, a PSPC connection line, and a NSPC connection line;

providing an P Side Programmable Current (PSPC) source having a PSPC input and a PSPC current line connected to said buffer through said PSPC connection line;

providing an N side (NS) latch adapted to receive an input of an N side control word and a N side write signal and outputs of N side switching signals; which are a function of said N side control word;

said NS latch providing outputs of N side switching signals which are a function of said N side control word, with outputs of said N side switching signals being provided to said input of said PSPC source;

providing an N Side Programmable Current (NSPC) source having an NSPC source input and an NSPC current line connected to said buffer through said NSPC connection line;

providing an P side (PS) latch adapted to receive an input of an P side control word and a P side write signal and outputs of P side switching signals, which are a function of said P side control word; and

said PS latch providing outputs of P side switching signals which are a function of said P side control word with said outputs of said N side switching signals being provided to said input of said PSPC source.

16. The method of claim 15 wherein said buffer control circuit includes a first inverter and a second inverter.

17. The method of claim 15 including:

providing said buffer control circuit with a first inverter and a second inverter each having an input and an output with said first having a first input and a first output and said second inverter having a second input and a second output;

providing for said first inverter to respond to said first PSPC source when said input signal transits from logic high to logic low to connect between said first PSPC source and said first output;

providing for said first inverter to respond to said second PSPC source when said input signal transits from logic low to logic high to connect between said second PSPC source and said first output;

connecting said first output of said first inverter to a node connected to said second input of said second inverter; and

said second inverter providing said output signal at said second output, from said second inverter.

18. The method of claim 15 including:

providing a PMOS FET and an NMOS FET in said first inverter having first ends of source drain circuits thereof connected to said output of said first inverter;

connecting said input to said first inverter to gate electrodes of said PMOS FET and said NMOS FET.

19. The method of claim 18 including connecting opposite ends of said source drain circuits of said PMOS FET and said NMOS FET to outputs of said first PSPC source and said second PSPC source.

20. A dual edge programmable delay unit comprising:

a buffer circuit which is adapted to receive a buffer input signal, said buffer input signal falling at an input signal fall time and said buffer input signal rising at an input signal rise time;

said buffer circuit being adapted to provide a falling buffer output signal at an output signal fall time and a rising buffer output signal at an output signal rise time;

a variable fall time control input;

a variable rise time control input;

a Fall Time Programmable Control Source (FTPCS) for programming a variable FTPCS signal to said buffer circuit as a function of said fall time control input;

a Rise Time Programmable Control Source (RTPCS) for programming a variable RTPCS signal to said buffer circuit as a function of said rise time control input;

said buffer circuit providing said buffer output signal with a fall time delay between said input signal fall time and said output signal fall time as a function of said variable FTPCS signal; and

said buffer circuit providing said buffer output signal with a rise time delay between said input signal rise time and said output signal rise time as a function of said variable RTPCS signal.